

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	(customiz\$4 development demonstration platform structured asic slice programmable processor high speed serdes fpga port driv\$4 test signal integrity electrical characteristic (IP or intellectual) pin\$4 link layer). clm.	USPAT	AND	ON	2006/12/08 15:01
S1	1141	(716/16-17).CCLS.	US-PGPUB; USPAT	OR	OFF	2006/12/08 11:53
S2	1	("6347395").PN.	US-PGPUB; USPAT	OR	OFF	2006/12/08 12:35
S3	10	"6347395".uref.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/12/08 12:26
S4	38	fpga and asic and (serdes (serializer near2 deserializer)) and port and slic\$3	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/12/08 12:40
S5	5	rapidslice	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/12/08 12:37
S6	1	asic same platform same serdes same slice	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/12/08 12:41
S7	1	("20060193346").PN.	US-PGPUB; USPAT	OR	OFF	2006/12/08 13:32
S8	0	structure\$2 asci fpga serdes port test (ip or (intellectual near3 property)) high near2 speed layer \$6slice	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/12/08 12:59
S9	0	structure\$2 asci fpga serdes port (ip or (intellectual near3 property)) high near2 speed layer \$6slice	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/12/08 13:00

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S10	0	structure\$2 asci fpga serdes port \$6slice	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/12/08 13:00
S11	9	structure\$2 asic fpga serdes port (ip or (intellectual near3 property)) high near2 speed layer \$6slice	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/12/08 13:03
S12	1163	(716/18).CCLS.	US-PGPUB; USPAT	OR	OFF	2006/12/08 13:05
S13	616254	asic slice platform custom	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/12/08 13:05
S14	51	asic slice platform custom\$6 serdes	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/12/08 13:06
S15	51	asic slice platform custom\$6 serdes (fpga or ((field or programmable or gate) near4 array))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/12/08 13:08
S16	103	asic platform custom\$6 serdes (fpga or ((field or programmable or gate) near4 array))	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/12/08 13:08
S17	52	S16 not S15	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	AND	ON	2006/12/08 13:20
S18	1	("20050183042").PN.	US-PGPUB; USPAT	OR	OFF	2006/12/08 13:20
S19	1	S18 and (prov\$3 near3 concept)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/12/08 13:26
S20	264	(asic same (prototyp\$4 or develop\$5)) and (fpga same external)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/12/08 13:27

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S21	34	(asic same (prototyp\$4 or develop\$5)) and (fpga same external) and slice	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/12/08 13:31
S22	1	(asic same (prototyp\$4 or develop\$5)) and (fpga same external) and slice and (serdes or gigablze)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/12/08 13:28

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With the introduction of ISSP2 **structured ASIC** devices, NEC Electronics builds on ... third-party **IP** vendors to **port** their **IP** cores to the ISSP **platform**. ...

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